Homework 4

Due Date: April 20

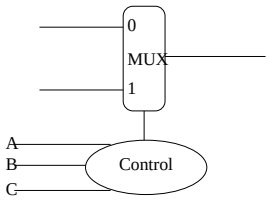
There is nothing to hand in for this homework assignment. There will be a short quiz at the **beginning of class** on the indicated date. The solution sheet will be posted on the course web page.

Do text problems (you may want to do the additional problems below **first**):

4.1, 4.5*, 4.7.1*-4.7.3*, 4.7.6*, 4.16.1-4.16.3

* Refer to Figure 4.17, which is a single-cycle data path. Also note that Figure 4.12 may have an error (depending on when your book was printed): The column labeled `ALU control input` should read `ALU control` **output**.

In addition:



Suppose a three-bit control signal determines the output of a two-input multiplexor, as shown above. If we call the three bits A, B, and C, assume line 1 (true) of the multiplexor is chosen if

`(((A OR B) OR C) OR (A AND C)) OR (A AND B).`

1. [5] Implement the logic for the control signal. Your circuit should directly implement the given expression (do not "optimize" it) using two-input AND and OR gates.
2. [5] Suppose the latency of an AND gate is 28ps (ps = picosecond) and the latency of an OR gate is 35ps. What is the length of the critical path of your circuit?