Homework 1 Solutions

1. μ represents microseconds = 10^{-6} seconds. Thus, $9.1792\mu\text{s} \times 10^{-6} = 0.0000091792\text{s}$. Since this is completely awkward, show the result in proper scientific notation:

   $9.1792\mu\text{s} = 9.1792 \times 10^{-6}\text{s}$.

   Similarly, $9.1792\mu\text{s} = 9.1792 \times 10^{3}$ ns.

2. The aspect ratio is 16:9.

3. Address generally refers to a location in memory/storage or a peripheral device. For example, every location in RAM is addressed by its byte (or even bit) position within the total number of bytes of the hardware.

4. Problems from text:

1.2 (a) assembly line → pipelining

(b) suspension bridge → dependability via redundancy. The answer here is **not** parallelism. Some suspension bridges happen to have cables arranged in a "parallel" way, but it's the redundancy that is important, not the arrangement.

(c) navigation systems → performance via prediction

(d) express elevators → make the common case fast

(e) library reserve desk → hierarchy of memories

(f) increasing gate area → parallelism. This means processing code in parallel using additional hardware.

(g) self-driving cars → abstraction to simplify design. For example, a company would generalize sensors for multiple uses.

1.4 (a) Here we are talking about storage, so use proper *binary* units ($2^{10}, 2^{20}$, etc.). Also remember that bits are represented by b and bytes by B.

$$\begin{aligned} \#B &= 1280 \times 1024 \times 3B/pixel \\ &= 3,932,160B \\ &= \frac{3,932,160}{2^{20}} \qquad (2^{20} = 1MiB) \\ &= 3.75MiB \end{aligned}$$

(b) Now we are talking about moving data/time; thus, this is not specific to storage, so use *metric* units ($10^3, 10^6$, etc.).

$$\begin{aligned} \#b &= 1280 \times 1024 \times 24b/pixel \\ &= 31,457,280b \\ \#s &= \frac{31,457,280}{100Mb} \\ &= \frac{31,457,280}{100,000,000} \\ &= 0.3145728s \end{aligned}$$

1.5 (a)

$$\begin{aligned} I/s &= \frac{CC/s}{CC/I} \\ &= \frac{I}{s} \\ P1 &= \frac{3 \times 10^9}{1.5} \\ &= 2 \times 10^9 \ I/s \end{aligned}$$

$$\begin{aligned} P2 &= \frac{2.5 \times 10^9}{1.0} \\ &= 2.5 \times 10^9 \ I/s \end{aligned}$$

$$\begin{aligned} P3 &= \frac{4.0 \times 10^9}{2.2} \\ &= 1.82 \times 10^9 \ I/s \end{aligned}$$

Thus, P2 has the highest performance using this metric.

(b)

$$\begin{aligned} T &= \frac{CC}{CR} \\ CC &= T \times CR \end{aligned}$$

$$\begin{aligned} T &= \frac{IC \times CPI}{CR} \\ IC &= \frac{T \times CR}{CPI} \end{aligned}$$

$$
\begin{aligned}
CC_{P1} &= 10 \times (3 \times 10^9) \\
&= 3.0 \times 10^{10} \\
IC_{P1} &= \frac{10 \times (3 \times 10^9)}{1.5} \\
&= 2.0 \times 10^{10}
\end{aligned}
$$

$$
\begin{aligned}
CC_{P2} &= 10 \times (2.5 \times 10^9) \\
&= 2.5 \times 10^{10} \\
IC_{P2} &= \frac{10 \times (2.5 \times 10^9)}{1.0} \\
&= 2.5 \times 10^{10}
\end{aligned}
$$

$$
\begin{aligned}
CC_{P3} &= 10 \times (4.0 \times 10^9) \\
&= 4.0 \times 10^{10} \\
IC_{P3} &= \frac{10 \times (4.0 \times 10^9)}{2.2} \\
&= 1.82 \times 10^{10}
\end{aligned}
$$

(c)

$$
\begin{aligned}
T &= \frac{IC \times CPI}{CR} \\
CR &= \frac{IC \times CPI}{T}
\end{aligned}
$$

$$
\begin{aligned}
CR_{P1} &= \frac{(1.0 \times 10^{10})(1.2)(1.5)}{7} \\
&= 5.14\ GHz
\end{aligned}
$$

$$
\begin{aligned}
CR_{P2} &= \frac{(2.5 \times 10^{10})(1.2)(1)}{7} \\
&= 4.29\ GHz
\end{aligned}
$$

$$
\begin{aligned}
CR_{P3} &= \frac{(1.82 \times 10^{10})(1.2)(2.2)}{7} \\
&= 6.86\ GHz
\end{aligned}
$$

1.7 (a) Be sure to answer the entire question.
Note 1: "clock cycle time" = clock period (CP) = $\frac{1}{CR}$.
Note 2: The GHz ratings are changed from the text; see footnote on HW sheet.

Proc.	CR	A	B	C	D
P1	2.6 GHz	1	2	3	3
P2	2.9 GHz	2	2	2	2

$$\begin{aligned} CPI_{P1} &= 1 \times 0.1 + 2 \times 0.2 + 3 \times 0.5 + 3 \times 0.2 \\ &= 2.6 \end{aligned}$$

$$\begin{aligned} CPI_{P2} &= 2 \times 0.1 + 2 \times 0.2 + 2 \times 0.5 + 2 \times 0.2 \\ &= 2.0 \end{aligned}$$

(b)

$$\begin{aligned} CC &= \sum(CPI_i \times IC_i) \\ CC_{P1} &= 1 \times 100,000 + 2 \times 200,000 + 3 \times 500,000 + 3 \times 200,000 \\ &= 2,600,000 \\ &= 2.6 \times 10^6 \end{aligned}$$

$$CC_{P2} = 2.0 \times 10^6$$

No calculations are necessary for CC_{P2} since the CPI is the same for all classes. Now there is still the question to answer: Which processor is faster?

$$\begin{aligned} T &= \frac{IC \times CPI}{CR} \\ &= \frac{CC}{CR} \\ T_{P1} &= \frac{2.6 \times 10^6}{2.6 \times 10^9} \\ &= 1.0 \times 10^{-3} \\ &= 1.0ms \\ T_{P2} &= \frac{2.0 \times 10^6}{2.9 \times 10^9} \\ &= 0.69 \times 10^{-3} \\ &= 0.69ms \end{aligned}$$

Thus, P2 is faster.

1.8 (c)

Compiler	IC	T
A	1×10^9	1.1 s
B	1.2×10^9	1.5 s

$$\begin{aligned} S &= \frac{T_{slow}}{T_{fast}} \\ T &= \frac{IC \times CPI}{CR} \end{aligned}$$

There are two approaches to this problem. One is as follows:
From part (a), the clock cycle time (period) is 1ns which makes $CR = 1$ GHz.

$$\begin{aligned} CPI_A &= \frac{T \times CR}{IC} \\ &= 1.1 \\ CPI_B &= \frac{T \times CR}{IC} \\ &= 1.25 \end{aligned}$$

Substituting T into the speedup formula:

$$\begin{aligned} S &= \frac{\frac{IC_{slow} \times CPI_{slow}}{CR}}{\frac{IC_{fast} \times CPI_{fast}}{CR}} \\ &= \frac{IC_{slow} \times CPI_{slow}}{IC_{fast} \times CPI_{fast}} \end{aligned}$$

Now find speedup of new compiler vs. A:

$$\begin{aligned} S &= \frac{IC_A \times CPI_A}{IC_{new} \times CPI_{new}} \\ &= \frac{1 \times 10^9 \times 1.1}{6 \times 10^8 \times 1.1} \\ &= 1.67 \end{aligned}$$

And finally the speedup of new compiler vs. B:

$$\begin{aligned} S &= \frac{IC_B \times CPI_B}{IC_{new} \times CPI_{new}} \\ &= \frac{1.2 \times 10^9 \times 1.25}{6 \times 10^8 \times 1.1} \\ &= 2.27 \end{aligned}$$

Another way to get the same answers is to find the time for the new process, and then use that in the speedup formula.

1.10.1 For one processor:

$$\begin{aligned} T &= \frac{IC \times CPI}{CR} \\ &= \frac{(2.56 \times 10^9 \times 1) + (1.28 \times 10^9 \times 12) + (256 \times 10^6 \times 5)}{2 \times 10^9} \\ &= 9.6s \end{aligned}$$

For two processors:

$$\begin{aligned} T_2 &= \frac{(\frac{2.56 \times 10^9}{1.4} \times 1) + (\frac{1.28 \times 10^9}{1.4} \times 12) + (256 \times 10^6 \times 5)}{2 \times 10^9} \\ &= 7.04s \end{aligned}$$

The speedup for two processors is then:

$$\begin{aligned} S &= \frac{T_{slow}}{T_{fast}} \\ &= \frac{9.6}{7.04} \\ &= 1.36 \end{aligned}$$

Note that even though we have two processors, the speedup is far from double. Similarly, the speedup with 4 processors is 2.5 and for 8 processors 4.29.

1.12.1

$$\begin{aligned} T &= \frac{IC \times CPI}{CR} \\ CPI &= \frac{T}{IC \times CC} \\ &= \frac{750}{(2.389 \times 10^{12}) \times (0.333 \times 10^{-9})} \\ &= 0.94 \end{aligned}$$

1.12.2

$$\begin{aligned} SPEC_{ratio} &= \frac{T_{ref}}{T} \\ &= \frac{9650}{750} \\ &= 12.87 \end{aligned}$$

1.12.3

$$\begin{aligned} T &= IC \times CPI \times 1.1 \times CC \\ &= 0.94 \times 2.6279 \times 10^{12} \times 0.333 \times 10^{-9} \\ &= 822.585s \\ &\approx 823s \end{aligned}$$

which is very close to a 10% increase, which makes sense.

1.13.1 This is a very basic calculation for CPU time. $T_1 = 1.125s$ and $T_2 = 0.25s$. Thus P2 is faster and has better performance.

1.13.4

$$MFLOPS = \frac{No.\ FP\ ops \times 10^{-6}}{T}$$

$$\begin{aligned} MFLOPS_{P1} &= \frac{(0.4 \times 5 \times 10^9) \times 10^{-6}}{1.125} \\ &= 1.78 \times 10^3 \\ &= 1.78\ GFLOPS \end{aligned}$$

$$\begin{aligned} MFLOPS_{P2} &= \frac{(0.4 \times 1 \times 10^9) \times 10^{-6}}{0.12} \\ &= 1.60 \times 10^3 \\ &= 1.60\ GFLOPS \end{aligned}$$

This indicates that P1 has a higher MFLOPS rating, but 1.13.1 shows that P2 is actually faster. Note that GFLOPS is a better unit in this case, although the question specifically asked for MFLOPS.